10-MBd High-Speed Optocoupler Design Guide

Introduction

Optocouplers are popularly perceived as being “slow” and are thus excluded from many designs in which they could potentially serve as excellent solutions to difficult design challenges. These solutions include enhancing noise immunity, protection against EMI emissions, ground-loop control, and safety isolation. At one time, when the only optocoupler options were discrete BJT phototransistors, this reputation for low speed was well earned; however, today’s optocouplers can attain switching speeds in the single digit nanosecond range.

The speed of “standard couplers” has been limited traditionally by the limitations of phototransistors and their associated large Miller capacitances. The simplest way to reduce the switching speed of standard BJT couplers is to optimize the drive and load values. There are other techniques that can be employed in reducing the switching time of standard coupler. The most extreme of these is to use the phototransistor as a photodiode, as shown in Figure 1.

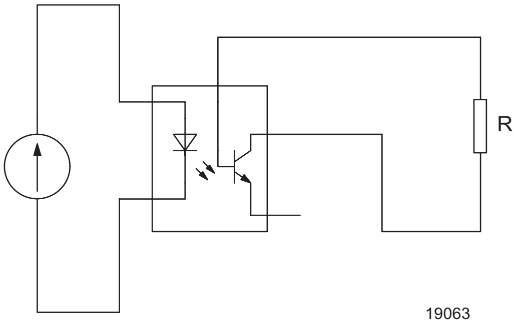


Figure 1. Photodiode detector configuration

An obvious improvement upon the simple photodiode detector configuration of the standard BJT phototransistor illustrated in Figure 1 is the circuit in Figure 2. Here, a transimpedance amplifier is added to the simple photodiode detector configuration.

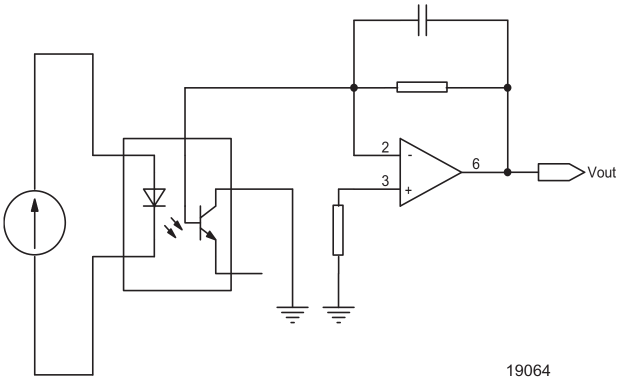


Figure 2. Transimpedance amplifier coupled photodiode

With this addition, the point is reached at which the switching performance of a “standard” coupler can be improved no further. Beyond this point, it becomes more economical to go to a device that is inherently capable of much higher switching performance. Even so, the basis for higher-speed optocouplers remains the circuit illustrated in Figure 2. In fact, all “high-speed” optocouplers are more sophisticated versions of this simple photodiode detector circuit, in conjunction with a transimpedance amplifier and an accompanying complementary output stage.

High-Speed Coupler Circuit Description

The basic internal architecture of the 10-MBd coupler is illustrated in Figure 3.

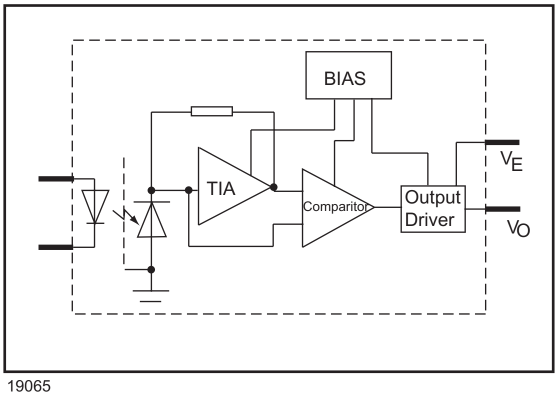


Figure 3. 10-MBd coupler Functional Diagram

Functionally, the circuit illustrated above represents an incremental improvement over a standard photodiode transimpedance amplifier coupled device. It is possible to build a discrete solution with similar performance; however, “the devil is in the details” and the actual design is far more involved than what is described above. A high-speed coupler is a very compact and simplified solution in comparison to the discrete approach. Vishay’s 10-Mbd couplers are built using an over/under double-molded construction technique, which gives results in superior optical transfer efficiency. A Gallium Aluminum Arsenide process ensures a fast input LED, but the designer still must take proper steps to insure that the LED is driven at an appropriate current level and speed. Other than its improved speed performance, this LED is similar to the one used in most of the other Vishay optocoupler products.

An important feature has been added between the input and output of the 10-MBd device: an ITO transparent and conductive shield. This vastly improves the common-mode noise immunity of the device, as measured by the performance parameter CMTR. This parameter is given in terms of slew rate in voltage between the primary and secondary side of the device. Currently, Vishay parts easily meet the industry standard for similar devices and boast a CMTR rate of 10 kV/µs.

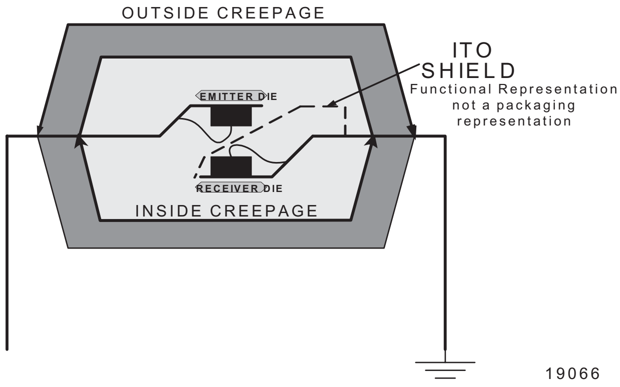


Figure 4. ITO shield implementation

Common-mode noise immunity is especially important to those designs that are operating at high edge rates, where even small coupling capacitances from primary to secondary can constitute significant coupling impedances. Consequently, choosing a high-speed part with the highest possible CMTR is crucial to such applications.

Package Types

The Vishay family of 10-MBd optocouplers is available in both surface-mount and DIP packaging options, as well as dual- or single-channel options. The devices are also available with several lead bend options, to meet specific creepage spacing requirements. Please refer to the 6N137/SHF67XX datasheet for more detailed option ordering information.

Bits and Bauds

The most obvious performance parameter to consider is the “bit rate,” which is more accurately evaluated in terms of “baud rate.” Therefore this is an opportune time to quickly review the concept of “baud rate.” This term was inherited from the days of early telephone systems and is still with us today. Yet, for meaningful comparisons, baud rate it is still the best way to proceed.

Many suppliers use bits/second to quantify data rate, but this approach can be misleading. A bit is an arbitrary term that can differ from one communication protocol to another. For example, a bit can be defined as two high-to-low transitions, followed by one low-to-high transition, followed by another two high-to-low transitions. The definition of what is a bit is totally arbitrary. Frequency is a better measure of data rate, but its use assumes a 50 % duty cycle condition, and this may not always be the case. Baud rate, on the other hand, is far more precise.

One baud refers to a signal transition from one state to another, whether it be high to low or low to high, without any recovery. Consequently baud rate is totally independent of communication protocol and duty cycle assumptions.

Figure 5 illustrates the concept of baud rate versus bit rate frequency.

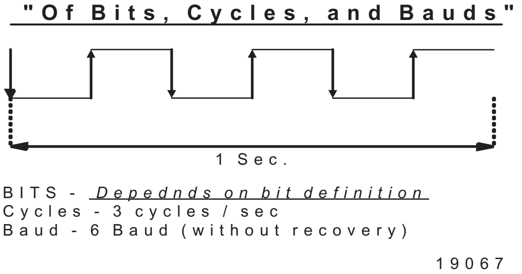


Figure 5.

Delay Time Performance

The best way to get a qualitative feeling for the switching time performance of a high speed 10-MBd coupler is to compare it with a standard coupler under similar conditions. Figures 6 and 7 provide just such a comparison. Figure 6 is a standard BJT optocoupler with a nominal input drive current of 10 mA and a nominal output load of 1 kilohm. Figure 7 represents the output of a 10-MBd high speed device under similar conditions.

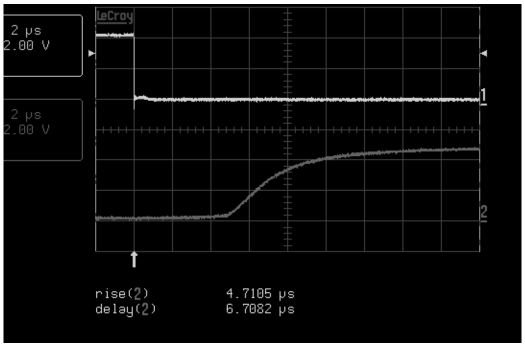
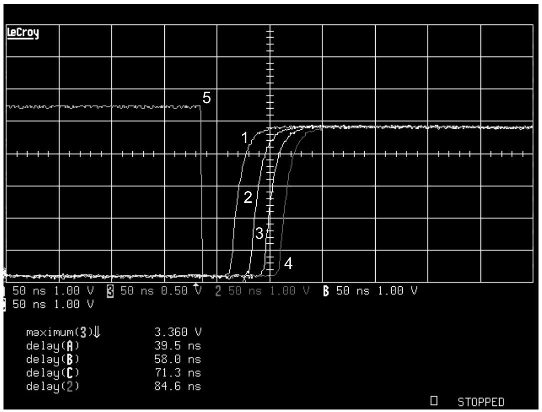


Figure 6. BJT switching performance @ I_F = 10 mA and R1 = 1 kilohm



trace 1	I_F = 3 mA	39.5 ns
trace 2	I_F = 5 mA	58.0 ns
trace 3	I_F = 10 mA	71.3 ns
trace 4	I_F = 18 mA	84.6 ns
trace 5	LED current	

Figure 7. 10-MBd switching performance with R1 of 1 kilohm

The performance factors associated with propagation delay are similar to what one would expect in a “standard” bipolar coupler: temperature, LED drive current, and load resistance. The only real difference is one of magnitude. For the purpose of this discussion and the rest of this document the circuit that shall be discussed is the one described below in Figure 8.

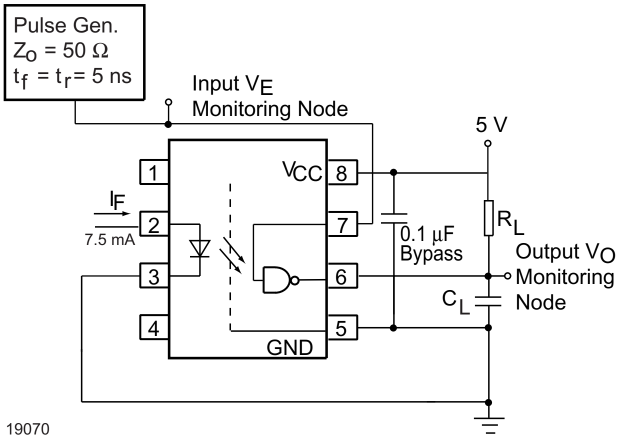
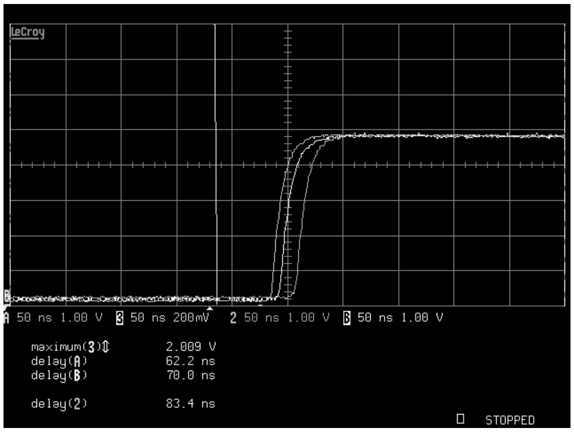


Figure 8. Propagation delay test circuit

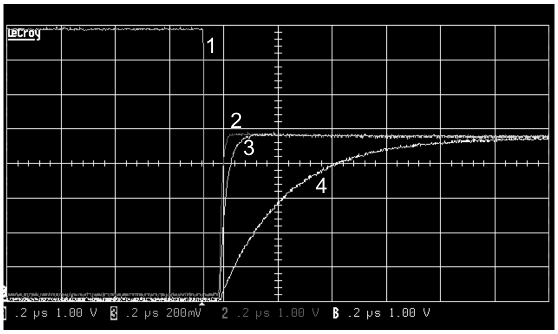
The relationship between temperature propagation delay and temperature is the same for 10-MBd couplers as for standard devices. The propagation delay has a positive temperature coefficient as seen from the scope data illustrated in Figure 9; but the absolute delays involved are in tens of nanoseconds rather than the tens of microseconds which are typical in standard couplers.



- 20 °C	62.2 ns
+ 25 °C	70.0 ns
+ 100 °C	83.4 ns

Figure 9. -20 °C, 25 °C, and 100 °C left to right

Propagation delay is also affected by load resistance, and in the same way as in standard couplers. As the load resistance increases, so does the turn-off time. This relationship is illustrated in Figure 10.



trace 1	input current
trace 2	300 ohm
trace 3	1 kilohm
trace 4	10 kilohm

Figure 10. Turn-off time vs. RL

The rules that govern the standard coupler with respect to turn-on time also apply to the 10-MBd couplers. As the drive current for the LED increases, so will the turn-on time, since the turn-on time is proportional to how much photocurrent is generated by the LED. One additional consideration that needs to be taken into account when discussing propagation delay is the input capacitance of the load. Load capacitance affects high-speed coupler switching speeds in much the same way that it affects a MOSFET driver, driving a capacitive load. The key question here is how long it takes to charge a capacitor with a constant current source. Consequently, the governing equations are the basic capacitance equation:

$Q = CV$

and the basic definition for current,

$I = Q/\Delta t$

Pulsewidth Distortion

In addition to propagation delay, an equally important parameter in some applications is pulsewidth distortion (PWD). This is mainly a measure of how asymmetric a pulse can be. Again, compared to a simple bipolar coupler, the pulse asymmetry associated with the turn-on and turn-off for a 10-MBd coupler is negligible. However, it must be taken into account in a worst-case analysis.

The first thing to consider is how we measure PWD. This is defined as the difference between the rise time T_{phl} and T_{plh}. The practical significance of this parameter is that it determines the maximum data rate which the part is capable of achieving. In other words the results of PWD are very similar to the effects of clock jitter on the data line. PWD is a small fraction of the measured rise time, but there will be slight changes in PWD performance with variations in LED drive current and ambient temperature.

High-Speed Rise Time Measurement

Designers used to the measurement of “high-speed” digital circuits may not imagine that measuring the speed of a 10-MBd device could be a challenging task. After all, even the cheapest oscilloscope probes offer bandwidths well into the hundreds of megahertz. When dealing with transient waveforms, however, the bandwidth of the required measurement probe is not the fundamental frequency of the signal in question but rather the rise time of the pulse. A novice engineer with a “faster is better” approach might design a system with a 1-MHz clock and a 2-psec rise time. If one were to measure this with a 500-MHz scope probe, it would seem more than adequate for a 1-MHz signal; however, the reality is that with a 2-psec rise time our 500-MHz probe would not have a chance to capture the actual signal waveform.

At 3 ns, a 300-MHz passive probe could start to approach bandwidth limitation-driven aliasing. More important than bandwidth limitations could be signal interface at the probe tip. The tip of the scope probe is not a simple RC circuit but more accurately an RLC, and the ringing of a transient excitation such as a square wave will be determined by the Q of the circuit, which increases with the size of L and decreases with R. By far the greatest contributor to probe inductance is the familiar ground LED on the typical oscilloscope probe. Aside from being an excellent source of noise pick-up, the loop area that it forms can contribute a significance lead inductance. Consequently, the measurement setup in Figure 11 offers the best approach short of using expensive and highly destructible active probes.

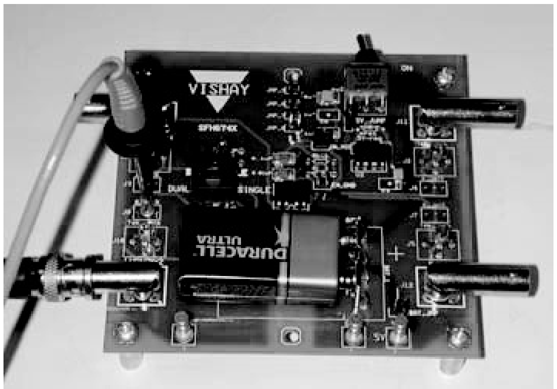


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Figure 11.

Board Layout Considerations

The same rules that govern high-speed board layouts govern the design of boards using 10-MBd couplers, with the added caveat that in the latter case one has isolation and safety concerns to deal with.

As in the case of all digital ICs, good decoupling is a must. It is recommended that a designer use an appropriately characterized capacitor, with excellent high-frequency response and low ESR.

An SMD ceramic bypass capacitor of approximately 0.1 µF in value is recommended. Should it be required to use leaded components, leads should be kept as short as possible to minimize lead inductance. A continuous ground plane is ideal for providing a low-impedance signal return path, as well as generating the lowest EMI signature by reducing phenomena such as unintended current loops. Should a continuous ground plane not be possible, it is important to minimize the length of the trace connecting V_{CC} and Ground. Furthermore, V_{CC} and the return trace should mirror each other on opposite sides of the board, thus creating the least effective impedance path for signal current. The preferred and less-preferred alternatives to PCB layout are described in Figure 12 and Figure 13.

In addition to signal integrity issues, safety isolation is often a primary consideration in PCB layouts. Without going into details beyond the scope of this document, a brief summary of practical PCB layout practices involves the following issues:

Vishay 10-MBd couplers meet reinforced insulation standards as specified by the testing approach described in IEC60950. This makes it possible to use the couplers for safety insulation wherever reinforced or double insulation devices would be called for, assuming that proper steps are taken to current limit the optocoupler in such a way that its inherent dielectric integrity is not compromised. For further information on reinforced insulation criteria please refer to the Vishay application note on Designing for Safety Agency Compliance.

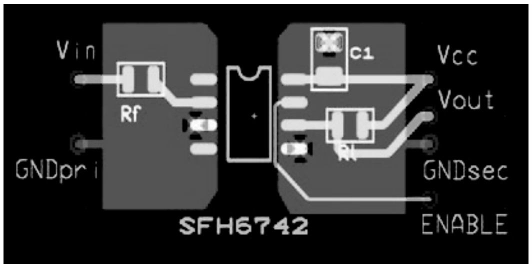

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Figure 12.

In addition to meeting reinforced insulation criteria, a proper design may often have to meet specified “creepage” and “clearance” criteria. Creepage and clearance requirements are determined by the end-use device specifications, and these can range from IEC60950 for information technology equipment to the rigorous IEC601-1 standard for patient connected medical equipment.

Clearance is fairly straightforward and is defined as the lengh of a gap across air between two conductors. The only factor affecting clearance distance is altitude above sea level, and unless one is involved in non-pressurized aircraft applications, this is not usually a major concern. Creepage, on the other hand, is a bit more involved. It includes several factors described below:

1. material CTI numbers
2. pollution degree
3. working voltage
4. particular safety standard

Pollution degree is often one of the most difficult issues to deal with, because designers must often assume a worst-case condition for this factor. One way to deal with this factor is to conformally coat the board in question, an expensive and troublesome process. A better approach is to cut a slot in the board. This has the effect of removing the creepage requirement along the board and replacing it with a clearance requirement along the air gap of the slot.

It must be kept in mind when taking this approach that the creepage distance along the body of the IC package itself must still be taken into account.

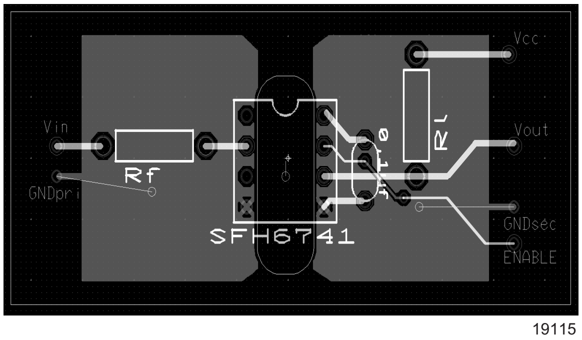
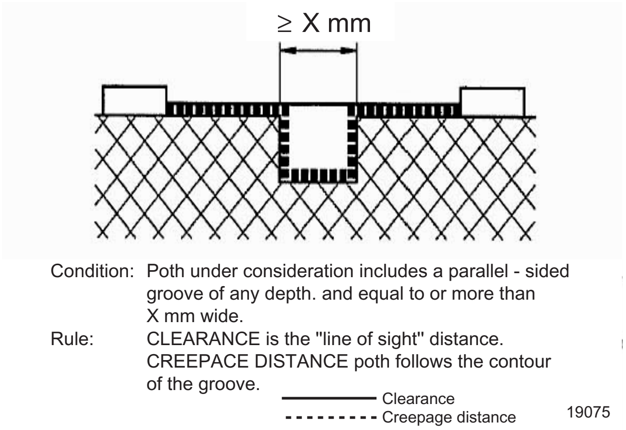


Figure 13.

Through-hole layout with slot cut into board



Condition: Poth under consideration includes a parallel - sided groove of any depth. and equal to or more than X mm wide.

Rule: CLEARANCE is the "line of sight" distance. CREEPACE DISTANCE poth follows the contour of the groove.

Figure 14. Creepage and clearance

High-Speed Coupler Solutions

Safety is by far the best understood application of optical isolation, and in the case of 10-MBd optocouplers this application remains an important but not exclusive target for this product. In most systems, safety is handled at the power supply end of the business, and from there on everything else falls under the low-voltage category.

Power Supply Safety Isolation:

High-speed optocouplers are gaining wider acceptance as power supplies migrate from the strictly analog world to a more digital approach. Increasingly, as microprocessors become less expensive, they are finding their way into a greater number of power supplies. At first their uses were limited to simple housekeeping and monitoring operations, requiring little data transmission bandwidth; however, the uses of on-board microcontrollers have now become more sophisticated, to the point where designers are seriously considering the use of “digital power control” in more power control applications. At first this trend was limited exclusively to the university lab, then to the high-end commercial market. Recently with the ever increasing affordability of high-performance embedded computational platforms such as DSPs, the lower end of the power supply market is beginning to stand up and take notice.

The digital approach requires the transfer of serial data across an electrical isolation barrier at a relatively high rate of speed. Figure 15 is the standard analog approach to power supply control, while Figure 16 adopts a more innovative secondary side control approach.

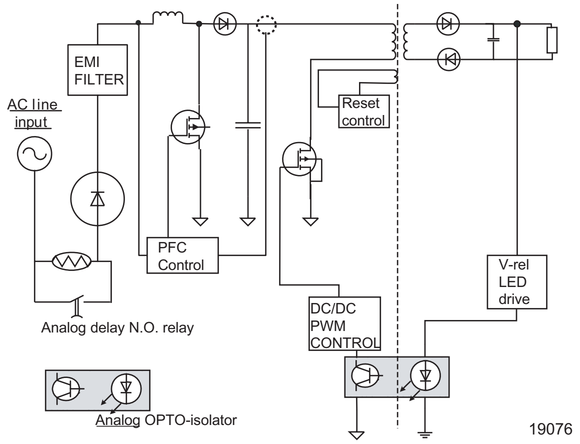


Figure 15. Typical Analog PSM Design

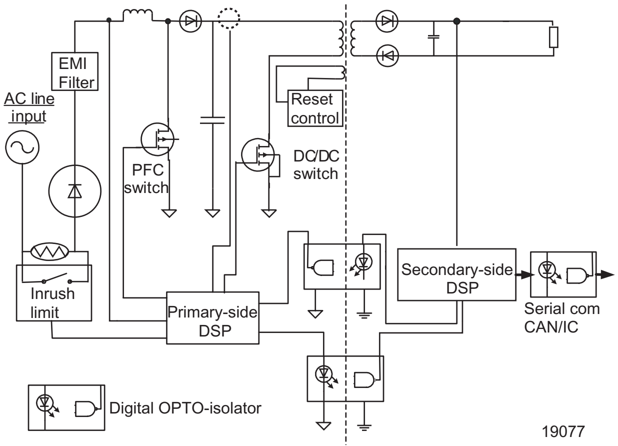


Figure 16. Typical Digital PSM Design

Figure 16 in fact represents the reality of many commercial power supplies today. A primary side controller for housekeeping functions such as high line voltage monitoring and inrush current limiting is a common feature in many power supplies. This usually requires some kind of communication link to the low-voltage side of the system, and a relatively high-speed coupler is often required for this application.

The purpose of the communication could be as simple as forwarding alarm information to the outside world.

As the prices of embedded processors continue to decrease, many designers have found it easier to include a dedicated microcontroller on both the input and output, with the connection between the two consisting of a bidirectional serial interface. Thus a two-microcontroller solution is often the most effective and economical approach to digital control.

Robust High-Speed Serial Communications:

As IT becomes a more dominant aspect of manufacturing and process control, so does the requirement for high-speed serial communications. Industrial/process control environments are especially challenging from a system design perspective in that they combine the worst of both worlds, demanding high-accuracy measurements in a worst-case safety and electrical noise environment. This necessitates the extensive adoption of electrical isolation throughout industrial control systems. Ethernet is quickly encroaching into the realm of industrial control, but the bulk of the first tier communications is still dominated by the various field bus technologies widely available in the market today. These are all implemented using some form of RS485 differential serial communications as illustrated in Figure17.

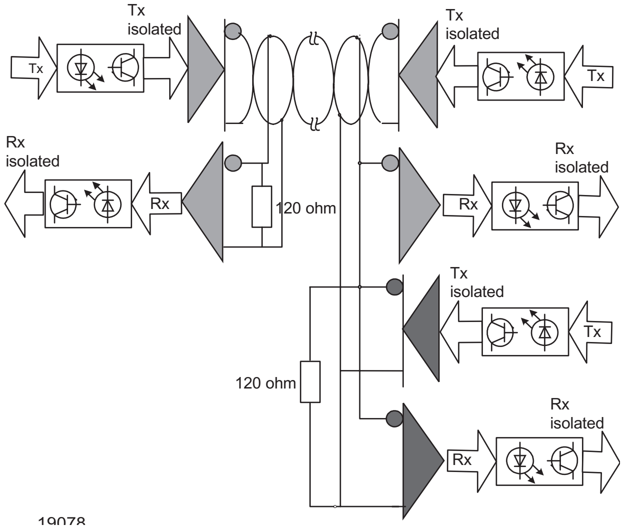


Figure 17. Isolated Industrial RS-485

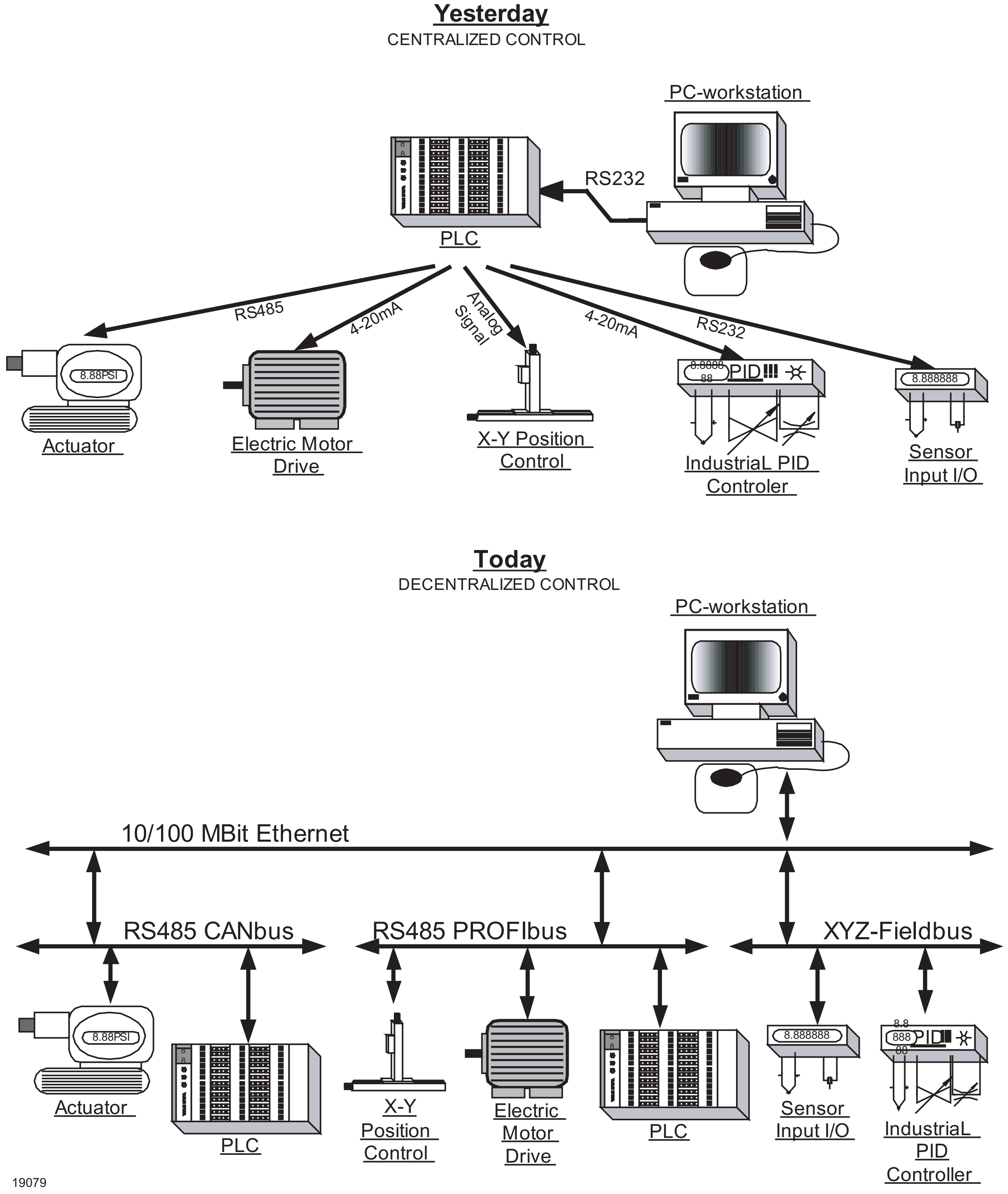
Field buses vary from manufacturer to manufacturer, but most are based on RS485 differential serial communications. Thus, regardless of the field bus topology they use, the requirement for isolation remains constant. This requirement is driven by these objectives:

1. Ground loop elimination
2. Common-mode noise isolation
3. DC reference level recovery
4. EMI reduction
5. Safety isolation

Industrial process control inevitably involves sending data across long distances, often under the worst possible conditions of RF interference. Moreover, these long distances often need to be covered with industrial RS485 serial communications. Without galvanic isolation, unpredictable current loops can be created. Common-mode noise is also a major concern in many industrial environments, especially as more switchmode solutions are replacing linear power handling approaches. Thus, the 10-MBd coupler's high CMR of greater than 10 kV/µs provides a very effective method of preventing common-mode sources from coupling onto sensitive instrumentation.

Since it is often difficult to “tie down” the ground reference rails of widely dispersed industrial automation systems with a low-impedance connection, significant voltage differences can develop between the ground reference of one system and another system several hundred feet away. These voltage differences can make it impossible for effective serial communication to be implemented without some type of isolation. Here again, optoisolation provides a very effective way to deal with this issue.

The advent of field bus topologies such as PROFIBUS and CANBUS has made the need for isolation even more critical. At first the communications from process to controller was a point-to-point connection. This centralized control structure added a certain level of simplicity to control systems, and limited the possibility of adverse component interactions. Now the advent of IT incursion into the industrial environment, coupled with field bus topologies, has removed whatever limits there might have been to the size of decentralized industrial control systems. Without isolation, therefore, the consequences of undesired component interaction would be impossible to predict or control.


Yesterday
CENTRALIZED CONTROL
PC-workstation
RS232
PLC
RS485
4-20mA
Analog Signal
4-20mA
RS232
8.88PSI
Actuator
Electric Motor Drive
X-Y Position Control
8.8888 88
PID
Industrial PID Controler
8.888888
Sensor Input I/O
Today
DECENTRALIZED CONTROL
PC-workstation
10/100 MBit Ethernet
RS485 CANbus
RS485 PROFIbus
XYZ-Fieldbus
8.88PSI
Actuator
PLC
X-Y Position Control
Electric Motor Drive
PLC
8.888888
Sensor Input I/O
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PID
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Figure 18.